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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,830	06/27/2003	Masaru Ozaki	027260-666	4828

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BURNS, DOANE, SWECKER & MATHIS, L.L.P.
P.O. Box 1404
Alexandria, VA 22313-1404

EXAMINER	
DINH, PAUL	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 01/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,830	OZAKI ET AL.	
	Examiner	Art Unit	
	Paul Dinh	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/27/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:
The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 4 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 4 is rejected because the limitation on lines 2-5 of claim 4 finds no clear support in the specification.

The following is a quotation of the second paragraph of 35 U.S.C. 112:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 is rejected because:

a. It is not clear that "the circuit" on line 8 means "a semiconductor integrated circuit (on line 1) or "a circuit" whose signal... (on line 7).

b. "closed circuit" is not clearly defined in the specification and claim 1.

c. It is unclear as to how "signal transfer characteristics are known".

Claims 2-6 are rejected because they depend on claim 1.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:
A person shall be entitled to a patent unless –

(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Luk et al (USP 5,883,814) who discloses and IC comprising:

(Claim 1) a variable region to be subjected to a layout modification in conjunction with a change of a circuit component within the variable region *(col 1 lines 56-60, col 2 lines 23-30, col 4 lines 22-33, 47-67, col 9 lines 33-37, 54-55, col 10 lines 42-43, variable region is the region with DRAM(s) that is subjected to a layout modification; circuit component within the variable region is one or more of: DRAM circuits/macros/components, DRAM memory capacity, DRAM configuration, DRAM structure, that is in conjunction with a change*); and

a fixed region (*is the region with controller (processor) or processor (logic) or logic processor in col 1-2 or processor/logic or system logic, logic macros/circuits) in col 5*) that is free from the layout modification in conjunction with the change of the circuit component within the variable region; and that includes a circuit (*a circuit is one or more of: processor, controller, logic macros/components/circuit, peripheral, registers, logic circuits (col 5), control unit/circuit (fig 4), I/O circuit (col 6))* whose signal transfer characteristics are known (*i.e., signal transfer characteristics are known by utilizing/performing one or more of: clock and timing analyzer, layout extraction, RC timing, circuit simulation, behavioral simulation, test pattern generation, synthesizers (all in fig 9), clock and timing verification (col 13 line 51), Assertion of timing, pin metal (in fig 14) and chip checking: DRC, LVS, TIMING(in fig 14)*) when the circuit is considered as closed circuit (*the circuit is considered a closed circuit, i.e., according to one or more of the followings: on-chip layout (title), system on a single integrated chip and integrated logic/DRAM chip (abstract, fig 8, 10-13), on chip interconnections (fig 2) instead of off chip interconnections (fig 1))*

(Claim 2) further comprising a newly added circuit component (*newly added circuit component is one or more of: decoder(s), I/O circuit(s), control circuit(s), peripheral circuit(s) in fig 6-7, also col 2 lines 27-30)* placed within the variable region.

(Claim 3) further comprising wiring for electrically connecting the circuit component in the variable region with the circuit in the fixed region, said wiring being disposed along a straight path connecting the circuit components (fig 2).

(Claim 4) wherein the layout modification leaves in the variable region an available region in which no circuit component is present, the circuit component in the variable region is

placed such that it fills the variable region extended by an amount of the available region *(see "layout of embedded, growable DRAM macros with different amount of memory capacity, banking" in col 1 lines 56-57, "layout method allow flexible addition of control logic macros/circuit to optimize ... memory chip layout" in col 2 lines 27-30, different variants of the integrated DRAM layout in fig 4B-D, and different ways the growable, flexible DRAMs layouted/integrated as shown in fig 6-8, 11-13 and taught in col 4-5, insofar the limitation is understood).*

(Claim 5) further comprising an anti-nose bypass capacitor provided to wiring between the variable region and fixed region (col 5 lines 44-48, col 8 lines 44-52, col 11 line 61 to col 12 line 4, fig 8, 11-12, 14).

(Claim 6) further comprising a newly added circuit component separately placed from the variable region and the fixed region (i.e., chip interface in fig 4A-D or I/O MUX in fig 8)

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is 571-272-1890. The examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Dinh
Patent Examiner

Paul Dinh
1/6/05